Review of Multilevel Inverters and Their Control Techniques

Ibrahim Emmanuel Tashiwa, Gyang Davou Dung, and Benson Stephen Adole

***Abstract*—Multi-level inverter is attaining higher AC power using a series of power semiconductor switches with numerous lower voltage DC sources to implement the power conversion by synthesizing a staircase voltage waveform. Sources like super capacitors, batteries, solar panels and other renewable energy voltage sources make up the multiple DC voltage sources. This work looks at the advantages and likely disadvantage of multi-level inverter, highlighting some of the shortfalls of existing inverter topologies while considering the effects of emerging Hybrid MLI Topologies. Hence this review paper proposes a distinctive seven level cascaded H-bridge multi-level inverter configuration in which the POD PWM technique is adopted. This design would potentially redress the problems inherent in other inverter circuit topologies reviewed.**

***Index Terms*—Inverter, Hybrid, Semiconductor, Topology, Multi-Level.**

I. Introduction

The concept of multi-level converters has been introduced since 1975 [1] and since then, being salient to manufacturer and researchers as a result of their merits over the traditional three level pulse width modulated inverters; gaining increasing attention in the area of high power and medium voltage applications in recent times. The key concept in a multi-level inverter is to achieve higher AC power using a series of power semiconductor switches with several lower voltage DC sources to perform the power conversion by synthesizing a staircase voltage waveform. Sources like super capacitors, batteries, solar panels and other renewable energy voltage sources constitute the multiple DC voltage sources. These types of inverters are suitable in high voltage and high-power applications due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltage with a limited maximum device rating. Hence, the paper reviews multi-level inverter topologies, control techniques, and applications.

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II. Multi-Level Inverters

Power conversion technology has been receiving increasing attention in the area of high power and medium voltage applications [2]. However, through contemporary research works, many innovative MLI topologies have been proposed in the past decades. Three of these topologies stand out as the major multi-level inverter topologies because they have been applied in industrial applications. These are;

i. Diode clamped (neutral-clamped) multi-level inverter [3]
ii. Capacitor clamped (flying capacitor) multi-level inverter [4]
iii. Cascaded Bridge multi-cell with separate dc sources [5]

These three topologies apply different mechanisms to produce the required output. Initially, cascaded MLI was developed and defined as a format, which connects separate DC-sourced full-bridge cells in series to give a staircase AC output voltage. Eventually, the cascaded inverter was manipulated with diodes blocking the sources to derive the diode-clamped or the neutral point clamped (NPC) multi-level inverter. Subsequently, the diode-clamped inverter was modified by replacing the diodes with capacitors to obtain the Flying capacitor (FC) or Capacitor clamped topology [6].

A. Diode Clamped or Neutral Point Clamped (NPC) MLI topology

The diode clamped MLI is also referred to as the Neutral Point Clamped (NPC) MLI because in its basic three-level structure, it has two diodes which clamp the switch voltage to half of the supply voltage and ensure that the supply voltage is equally shared between the two halves of the switches and held at these points with a neutral point between them. The mid-voltage level is defined as the neutral point. This type of MLI shown in Fig. 1 uses diodes to provide multiple voltage levels through the different phases of the capacitor banks which are in series. Because the NPC inverter effectively doubles the device voltage level without requiring precise voltage matching; its circuit topology prevailed in the 1980s. Also the application of the NPC inverter and its extension to multi-level converter was found in bridge converter [7].

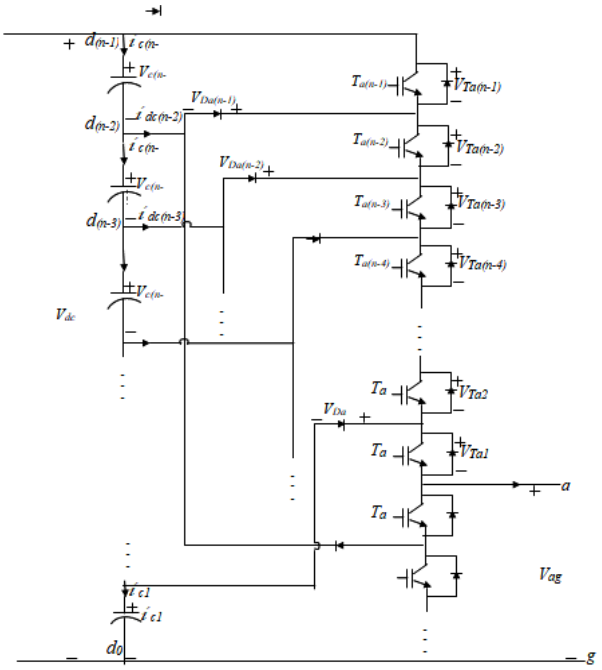

Fig. 1. The n-level Diode Clamped Multi-Level Inverter.

The advantages of the Diode Clamped multi-level inverter is all of the phases share a common dc bus, which minimizes the capacity requirement of the converter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back interconnection or an adjustable speed drive. The capacitors can be pre-charged as a group and this type of inverter provides high efficiency because it is the fundamental frequency that is used for all the switching devices and hence make it a simple method of the back to back power transfer systems.

The major drawback of this MLI topology is that the maximum output AC voltage is half of the input DC voltage. This problem can be solved by increasing the switches, diodes and capacitors. This leads to increase in circuit complexity and cost. The static and dynamic sharing of the voltage across the switches is difficult with some undesirable features such as fluctuations of the neutral point voltage due to the difference in the switching characteristics. It has over voltage problems and due to capacitor balancing issues, the practical implementation of this topology is limited to three levels. With a level higher than three, there is the necessity of a capacitor voltage balancing control circuit.

Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control. The number of clamping diodes required is quadratically related to the number of levels, which can be cumbersome for units with a high number of levels [8].

Diode clamp MLI is been applied in the following ways

i. Static VAR compensation: This technology is used to adjust the reactive power in a system so that the system's power factor is maintained within the desirable limits (near unity). It offers fast and smooth reactive power (VAR) compensation.
ii. They are used in Variable speed motor drives to control and maintain the speed, conserve energy and improve the lifespan of the drives.
iii. They are used for high voltage system inter connections.
iv. They can be interfaced with high voltage DC and AC transmission grid system [9]

B. Flying Capacitor Multi-level Inverter

This MLI topology was proposed by [3] to mitigate the problem of static and dynamic sharing of the voltage across the switches as inherent in the NPC topology. The structure and the switching states of this inverter is similar to that of the diode-clamped inverter, except that instead of using clamping diodes, the inverter uses capacitors in their place. The capacitors that replace the diodes in the diode clamped inverter structure are independent (flying) of the other capacitors in the circuit. These flying capacitors transfer limited amount of voltage to electrical devices. Hence, the circuit is called the flying capacitor (FC) inverter, with independent capacitors clamping the device voltage to one capacitor voltage level. This topology shown in Fig. 2 has a ladder structure of DC side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. It is called a flying capacitor (FC) inverter because the capacitors that replace the diodes in the diode clamped inverter are independent (flying) of the other capacitors.

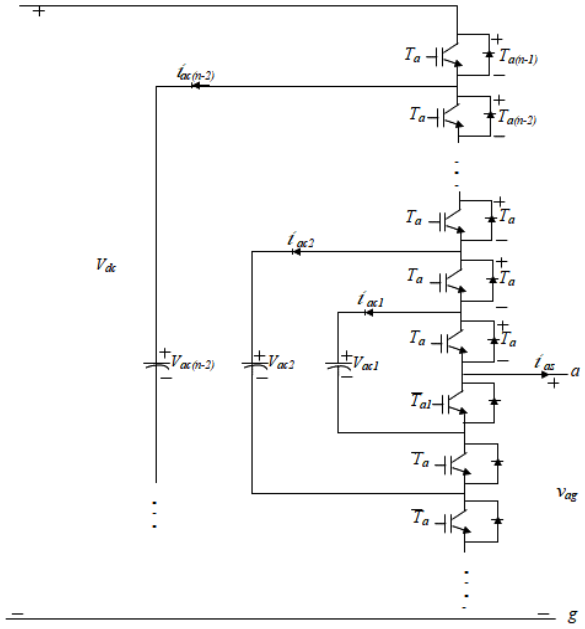

Fig. 2. The Generalized n-level Flying Capacitor Inverter.

The FC topology has several attractive properties in comparison with NPC inverters. Transformer less operation and redundant phase states that allow the switching stress to be equally distributed between semi-conductor switches with Phase redundancies available for balancing the voltage levels of the capacitors. It has redundancies for inner voltage levels; in other words, two or more valid switch combinations can synthesize an output voltage. The voltage synthesis in a capacitor clamped converter has more flexibility than a diode clamped converter.

Real and reactive power flow can be controlled. The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.

Although the FC MLI addresses the problem of the NPC, it is still inherent with some problems. These inverters require excessive number of storage capacitors for high voltage steps. This restricts high voltage application of the system with control that is complicated in tracking the voltage trace and the voltage levels for all of the capacitors. Also, pre-charging all of the capacitors to the same level and start up are complex.

Other drawback of this MLI topology is that the maximum output AC voltage is half of the input DC voltage just like the Diode clamped topology and it has switching redundancies hence its switching utilization and efficiency are poor for real power transmission. Due to high frequency switching, there are switching loses in the system and the large numbers of capacitors are both more expensive and bulky than clamping diodes in multi diode clamped inverters. Packaging is also more difficult in inverters with a high number of levels.

The flying capacitor multi-level inverters can be applied in;

i. Induction motor control using DTC (Direct Torque Control) circuits.
ii. Static Var generation.
iii. Both AC-DC and DC-AC conversion application
iv. Converters with harmonic Distortion capabilities.
v. Sinusoidal current rectifier.

C. Cascaded Multi-level (cascaded H-bridge) Inverter

Although the cascade inverter was invented earlier, its applications did not prevail until the mid-1990s. The rise of this technology to prominence follows the demand for higher power equipment which now reaches the megawatt level by industries. Due to the great demand of medium-voltage high power inverters, the cascade inverter has drawn tremendous interest ever since. Most of the MLI researches are carried out in the Cascaded topology. These are mostly modifications in its in-built structure, which have resulted in the evolution of renewed trends. Several patents of this topology were evolved for use in regenerative type motor drive applications [10]. Two major patents were filed to indicate the superiority of the cascade inverters for motor drive and utility applications. The last entry for U.S. multi-level inverter patents, which were defined as the capacitor-clamped multi-level inverters, came in the 1990s [11]. A version of the CHB multi-level inverters using standard three-phase two-level inverters was recently proposed [12]. Its circuit uses an output transformer to add the different voltages.

In recent times, these multi-level inverters are extensively used in high power applications with medium voltage levels. The field of applications includes use in laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on. In general, CHB MLIs may be subdivided into;

i. Symmetric CHB MLI: These are inverters in which the amplitude of all the isolated supply DC sources to each of the H-bridge cells is equal.
ii. Asymmetric CHB MLI: These are CHB MLIs in which at least one of the DC sources presents different amplitudes.
iii. Hybrid CHB MLI: Hybrid MLI technology implies that the converter is implemented with;

- Different semi-conductor device technology
- Different nature and amplitude of DC sources
- Hybrid modulation strategy [13]

Fig. 3 shows the generalized P2 multi-level inverter structure.

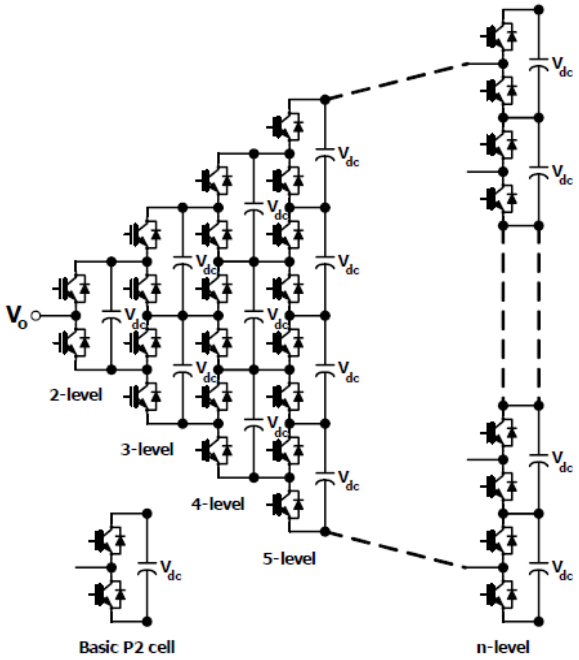

Fig. 3. Generalized P2 Multi-level Inverter Structure.

The Cascaded H-bridge MLI structure has become a very attractive solution for industrial application due to it modular structure which solves the problem of voltage imbalance found in the NPC and FC MLI topologies. The cascaded H-bridge inverter consists of power conversion cells, each supplied by an isolated dc source on the dc side, which can be obtained from batteries, fuel cells, or ultra-capacitors. The advantage of this topology is that the modulation, control, and protection requirements of each bridge are modular. It should be pointed out that, unlike the diode-clamped and flying-capacitor topologies, isolated dc sources are required for each cell in each phase. The absence of voltage imbalance is the main advantage of this MLI configuration and they are capable of handling higher voltages. Using the appropriate modulation scheme, they can be used to reduce and even eliminate common mode voltages. Common Mode Voltage is the voltage that appears in common at both input terminals of a device with respect to the output. These voltages generate common mode currents which in-turn produce electromagnetic interference, grid current distortion and additional losses in the system.

They synthesize a near sinusoidal output and smaller or even no output filter requirement. They require less number of components in each level compared to NPC and FC topologies. They do not require clamping diodes or flying capacitors and their load power is distributed among the switching devices so that they are not overloaded or over stressed.

The major setback of the cascaded H-bridge MLI topology is that, this approach requires many isolated DC sources and link voltage controllers.

MLIs yield voltages ranging from medium to high. They can be applied in various applications such as in RE sources,

industrial drives, laminators, blowers, fans and conveyors. Small voltage steps result in making the multi-level inverter withstand better voltage, fewer harmonics, high electromagnetic compatibility (EMC), reduced switching losses and better power quality [14].

III. Emerging Hybrid MLI Topologies

Multi-level inverters utilize power semi-conductor devices to convert several small DC sources directly to medium grid voltages (2.3, 3.3, 3.4, 4.16, or 6.9kV). Recently, several other hybrid families of ML inverters have emerged as a solution for working with higher voltage levels [15]. These hybrid multi-level converters are composed of different multi-level topologies with unequal values of DC voltage sources and different modulation techniques and/or semi-conductor technologies. Among these newer emerging multi-level inverter topologies are the;

i. Mixed-level Hybrid multi-level cells.
ii. Asymmetric Hybrid multi-level cells [16]
iii. Soft-switch multi-level inverters [17]

In all these emerging cascade MLI topologies, the key feature is the reduction of power circuit components, significant reduction in cost and/or DC sources when compared to the conventional configuration in the same voltage level category. However, the application of different multi-level topologies results in total loss of modularity and produces problems with switching frequency and restrictions on the modulation and control method [15].

A. *Mixed-level Hybrid Multi-level Cells*

The hybrid multi-level converters are composed of different multi-level topologies with unequal values of dc voltage sources and different modulation techniques and/or semiconductor technologies. The advantage of this topology is to reduce the amount of separate dc sources. With appropriate selection of switching devices, the converter cost is significantly reduced.

B. *Asymmetric Hybrid Multi-level Cells*

An asymmetric multi-level inverter is a multi-level converter fed by a set of DC voltage sources where the magnitude of at least one of the separate DC voltage sources are different or change dynamically. The main advantage of asymmetric multi-level converter is that it uses less number of semiconductor switches compared with symmetric topology. One interest of the asymmetric configuration is that the number of levels is higher with the same number of cells in the symmetric case, whereas it grows exponentially, in the asymmetric case. The asymmetric topology requires only twelve switches to obtain 7, 9, 15, 21 level output voltage [16].

Depending on the availability of dc sources, the voltage levels are not limited to a specific ratio. This feature allows more levels to be created in the output voltage, and thus reduces the harmonic contents with less cascaded cells required. Thus, these converters reduce the size and cost of the converter and improve the reliability since fewer semi-conductor switches and capacitors are employed.

C. *Soft-switched Multi-level Inverters*

There are numerous ways of implementing soft-switching methods to reduce the switching loss and to increase efficiency for different multi-level inverters. For the cascaded inverter, because each inverter cell is a two-level circuit, the implementation of soft switching is not at all different from that of conventional two-level inverters. For capacitor- or diode-clamped inverters, however, the choices of soft-switching circuit can be found with different circuit combinations. Although zero-current switching is possible, most literatures proposed zero-voltage-switching types including auxiliary resonant commutated pole (ARCP), couple inductor with zero-voltage transition (ZVT), and their combinations. Detailed soft-switching circuit operation for inner devices and outer devices can be found in [16].

IV. Control and Modulation Techniques for Multi-Level Inverters

One of the salient factors that determine the performance of cascaded multi-level inverters is the control or modulation techniques adopted.

Modulation refers to the process of varying one or more properties of a periodic waveform called the carrier signal with a modulating signal which typically contains information to be transmitted. In power electronic converters, modulation is the strategy of controlling the switching action of electronic devices from one state to the other by varying the properties of one waveform signal (carrier signal) using another waveform (reference Signal). Each family of power converter has a preferred modulation strategy associated with it so that it can optimize its circuit operation for the target criteria most appropriate for the family. Different control techniques exert different effects on different topologies of inverters. Some affect harmonics, others the voltage levels, yet, others the output power. The choice of the modulation strategy to be developed for a particular family of converters is predicated upon the following considerations;

i. Switching frequency.
ii. Distortion level.
iii. Losses.
iv. Harmonic generation.
v. Speed of response.

A number of unique modulation and control strategies have been developed and adopted for the efficient functioning of the multi-level inverter. The modulation methods used particularly in multi-level inverters can be classified according to switching frequency as shown in Fig. 4 [17].

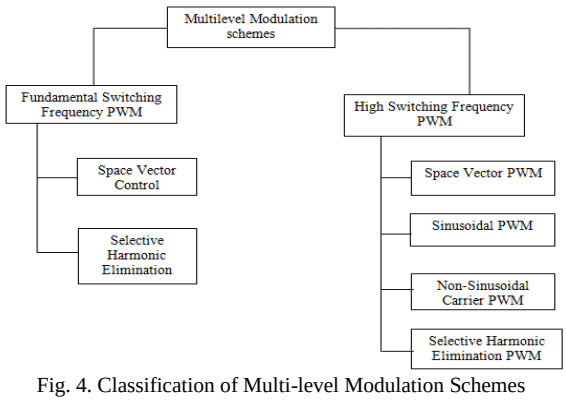

Fig. 4. Classification of Multi-level Modulation Schemes

Methods that work with high switching frequencies have many commutations for the power semiconductors in one period of the fundamental output voltage. A very popular method in industrial applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage. Another interesting modulation alternative is the Space Vector Modulation (SVM) strategy, which has been used in three-level inverters [18].

Furthermore, there are different control techniques available for a CHB MLI. Among all those techniques, PWM control technique, which produces less THD values, is most preferable. PWM is a technique of generating sinusoidal AC power from DC power sources in electronic power converters is by means of modifying the width of the pulses in a pulse train in direct proportion to a small control signal; the greater the control voltage, the wider the resulting pulses become. Thus, a dc voltage source can be made to look like an Ac signal across a load by altering the duty cycle of the PWM signal. The pattern at which the duty cycle of the PWM signal varies can be generated using simple analogue components, a digital microcontroller, or specific PWM integrated circuits. In PWM technique, modulated signal can be of pure sinusoidal, third harmonic injected signals and dead band signals.

Methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of output voltages, generating a staircase waveform. Representatives of this family are the multi-level selective harmonic elimination and the space-vector control (SVC) [19].

For generation of triggering pulses to the MLI, carrier signals are constructed for different modulation indices like APOD, POD, PD, PS and Hybrid control techniques. Thus, multi-level sinusoidal PWM can further be classified as shown in Fig. 5. Multi-carrier PWM techniques have sinusoidal signal as reference wave and triangular as carrier signals [20].

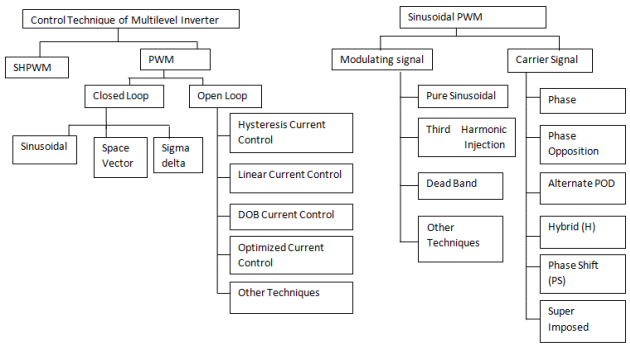

Fig. 5. Classification of Sinusoidal PWM

Application of these control techniques result in cascaded multi-level inverters synthesizing output voltages with very low THD. However, they do not take into account that cascaded inverter cells should equally share the overall output power.

V. Shortfalls of Existing Inverter Topologies

Most of the existing inverter topologies are limited because;

i. They restrict high voltage applications of the inverter to single phase systems.
ii. Multi-level topologies were not incorporated.
iii. Where multi-level is applied, it is in most cases developed to at most five levels.
iv. Low power output and low power quality as a result of higher THD.
v. High switching losses.
vi. Poor switching utilization and efficiency.
vii. Control complexity.
viii. Constrains of device rating for high frequency switching.
ix. Circuit complexity that comes with multi-level requirements. Voltage imbalance problems i.e. Problems arising from unbalance/unequal distribution of the switching losses among the constituting semi-conductor switches, which is a consequence of firing the switches averagely with different sequence of gate signals.
x. High harmonic distortions i.e. poor quality of output Voltage and current waveforms.
xi. High cost of implementation and procurement.

VI. The Configuration Proposed in this Review Paper

This review paper proposes a unique seven level cascaded H-bridge multi-level inverter configuration in which the POD PWM technique is adopted. This design would potentially redress the problems inherent in other inverter circuit topologies reviewed .The circuit configuration, the operational principles and the switching functions of the inverter are unique.

Conventionally, an nth level voltage waveform can be obtained using the relationship;

(P=2n+1)

Where

P = Voltage levels

n = number of H- bridge modules

Table I depicts the obtainable output voltage levels and their corresponding number of H-bridge modules per phase in conventional CHB-MLI configuration.

TABLE I: Conventional Configuration of CHB-MLI Topologies

Levels (P)	No. of H-bridges (n)	No. of semi-conductor switches per phase (4n)	Three phase no. of SC switches (12n)	No. of H-bridges (for 3 phase)
3	1	4	12	3
5	2	8	24	6
7	3	12	36	9
9	4	16	48	12
11	5	20	60	15

The proposed choice of a 7-level MLI configuration is to avoid high complexity of the circuit, attain high power that can be utilized in industries and to ensure that the power quality has low THD levels. It consists of nine cascaded H-bridges. Each H-bridge comprises four power electronics switching devices and outputs three voltage levels $+V_{dc}$, 0 and-V_{dc}. so that when the three bridges are cascaded, seven steps of staircase waveforms are generated as shown in Fig. 6.

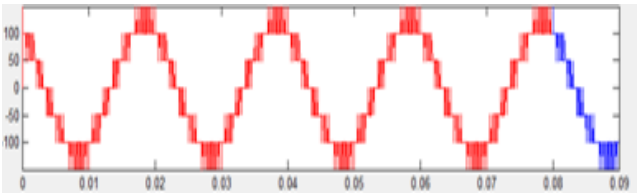

Fig. 6. Staircase Waveform of a 7-Level CHB Inverter.

Also, the Phase Opposition Disposition (POD) PWM technique is recommended for equitable load distribution among the switching devices. This would enhance efficiency and longevity of the devices. In the Phase POD technique, the carrier signals are aligned in symmetric mirror image above and below the zero reference axes. For a seven level MLI, six carrier signals are aligned in symmetric mirror images above and below the zero reference axes.

Typical comparative performance indices of the different carrier based SPWM techniques from literature are as shown in Table II.

TABLE II: PERFORMANCE INDICES OF THE DIFFERENT CARRIER BASED SPWM TECHNIQUES

PWM Technique	Symmetric Connection of7-Level Inverter (%)	Asymmetric Connection of 7-Level Inverter (%)
PD	24.6	21.84
POD	23.13	20.22
APOD	24.46	19.42

(From [20])

VII. CONCLUSION AND RECOMMENDATIONS

This paper presented a review of the MLI topologies, it controls mode and application. However, the key concept in a multi-level inverter is to achieve higher AC power using a series of power semiconductor switches with several lower voltage DC sources to perform the power conversion by synthesizing a staircase voltage waveform. Sources like super capacitors, batteries, solar panels and other viable renewable energy voltage sources constitute the multiple DC voltage sources.

Hence with the continual demand for higher voltages as applicable to some modern devices, modelling of advanced MLI such H-bridge multi-level inverter needs cognizance. Going forward, a future trend is to apply fiber-optic technologies for sensors, gate drive controllers and communication.

i. The inclusion of soft-starter elements across the MOSFET terminals at the H-bridge circuit is recommended in order to solve the problem of stability in the system.
ii. The use of microcontrollers to control the switching devices (MOSFETs) make for flexibility in desired outputs voltages and frequencies (110V or 220V, 60Hz or 50Hz), switching efficiency and a drastic reduction in circuit complexity and costs. A greater number of power semiconductor switches are being replaced by the micro controller.
iii. The introduction of a topology which incorporates the least number of voltage sources, semiconductor switches and gate triggering circuit which will ensure minimum switching losses, a further reduction in circuit size, complexity and installation cost could be explored.
iv. Optimization techniques based on Genetic Algorithm (GA) is proposed for computing switching angles only for the 7-level inverter.

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